SPECIFICATIONS

Model 2323A

INPUT

START: Bridged high impedance pair. Lemo-type connectors. Input trigger level adjustable over the range ±3 V via front-panel potentiometer, supplied at -400 ±50 mV with a negative-going edge. This input initiates the timing cycle.
STOP: Standard NIM input, Lemo-type connectors. This input terminates the timing cycle in the latched mode. Active in both latched and preset modes. The delay is < 20 nsec.
OR: Standard NIM input, Lemo-type connector. Input impedance 50 Ω. Produces outputs as long as the OR signal is asserted.
BLANK: Standard NIM input, Lemo-type connector. Input impedance 50 Ω. Cancels gate outputs as long as the BLANK signal is asserted. Overrides OR input.

OUTPUT

BUSY LED: Indicates unit is active.
NIM: Standard NIM (-16 mA) signal, Lemo-type connector. Goes low for gate duration. Rise time ≤ 2 nsec; fall time ≤ 2.5 nsec.
$\overline{\text{NIM}}$: Standard NIM (-16 mA) signal, Lemo-type connector. Goes high for gate duration. Rise time ≤ 2 nsec; fall time ≤ 2.5 nsec.
ECL: Complementary ECL levels, 2-pin connector. PC-mounted shorting plug allows this output to be logically identical to the GATE or DELAY pulse or their complements.
TTL: An FET open drain output (250 mA, 0.5 W maximum). PC-mounted shorting plug allows this output to be logically identical to the GATE or DELAY pulse or their complements.
DELAY: Standard NIM (-16 mA) signal, Lemo-type connector. Delayed from start of NIM by the gate width. (Goes low at trailing edge of gate.) Programmable for 10, 30, 100 or 300 nsec duration. Rise time ≤ 2 nsec.

GATE WIDTH

Range: 100 nsec to 10 sec (50 nsec width at reduced accuracy and stability).
Accuracy: ±0.2% of full scale.
Temperature Stability: < 200 ppm/°C.
Jitter: < 0.3% of setting.
Resolution: 0.1% of full scale.

DELAY WIDTH

Width Options: 10 nsec, 30 nsec, 100 nsec, 300 nsec.
Accuracy: ±20%.

GENERAL

Input-Output Delay: 24 nsec (Start input to NIM output).
Recovery Time: None. The unit may be retriggered any time after the timing cycle has been completed.
Packaging: Double-width module in conformance with CAMAC Standard; ESONE Report EUR4100 or IEEE Report #583. RF-shielded.
Power Requirements: 1.8 A at +6 V; 1.3 A at -6 V; 50 mA at +24 V; 75 mA at -24 V; 21.6 W total.

Model 4222

INPUT

Trigger Input (TRIG): Two bridged front-panel Lemo-type connectors; high input impedance, positive/negative edge selection via side-cover switch; threshold level adjustable between -1.5 V and +1.5 V with a front-panel potentiometer; 10X threshold monitor on front panel; minimum input width is 5 nsec; unused input must be terminated in 50 Ω.
Clear Input (CLR): Two bridged front-panel Lemo-type connectors; high input impedance accepts NIM level pulses; minimum input width is 50 nsec; unused input must be terminated in 50 Ω.
Clock Input (CK): Two bridged front-panel Lemo-type connectors; high input impedance, selected by internal strap; NIM level inputs; unused input must be terminated in 50 Ω. Clock input frequency must be 31.25 MHz ±0.1%. Stability determines the long-term accuracy of the time delays.

OUTPUT

BUSY and $\overline{\text{BUSY}}$ Outputs (B & $\overline{\text{B}}$): Two front-panel Lemo-type connectors; NIM level outputs. BUSY output state goes true in response to a valid Trigger and remains true until either the end of the shortest delay or the end of the longest delay as selected by an internal switch.
Delayed Level Outputs (OUT & $\overline{\text{OUT}}$): Two front-panel Lemo-type connectors per channel; NIM level outputs; both direct (OUT) and complementary ($\overline{\text{OUT}}$) outputs are provided. A set of side-panel switches permits the selection of either independent outputs or coupled window outputs:
- INDEPENDENT: 1, 2, 3, and 4:
  Each channel output (OUT) goes "true" when the corresponding programmed time delay has elapsed; output is reset by the Clear or by the next Trigger if the Retrigger Mode has been selected.
- COUPLED: 1 and 2, or 3 and 4:
  Channel 1 (3) output (OUT) goes "true" when time delay 1 (3) has elapsed and goes "false" when time delay 2 (4) has elapsed; delay 1 (3) < delay 2 (4). Channel 2 (4) output (OUT) goes "true" when delay 2 (4) has elapsed and is reset by Clear or by the next Trigger if the Retrigger Mode has been selected.

Delayed Pulse Output (P1-P4): One front-panel Lemo-type connector per channel. Each channel's PULSE OUT delivers a 1 nsec rise time 5 V pulse (into 50 Ω) when the corresponding time delay has elapsed; pulse width 100 nsec ±10%.

GENERAL

Delay Range: 170 nsec to 16.777215 msec in 1 nsec increments.
Accuracy: ±200 psec ± time base error.
Jitter: 150 psec R.M.S. maximum; up to 1 msec delay (see manual for additional information).
Insertion Delay: 170 nsec.

Crosstalk: < 500 psec when delays differ by less than 8 nsec, 0 otherwise.
Internal Time Base: High stability quartz oscillator:
$\Delta f/f_0$: $\pm 5 \cdot 10^{-6}$ initial frequency tolerance;
T_c : < 0.5 ppm/°C;
Aging : $< 3 \cdot 10^{-9}$/day.
Packaging: Single-width standard CAMAC module.
Power Requirements: 40 mA at +24 V; 1.3 A at +6 V; 2.5 A at -6 V; 130 mA at -24 V.

CAMAC COMMANDS

Model 2323A
Dual Programmable Gate and Delay Generator

CAMAC COMMANDS

C or Z: Stops channels A and B gates.

X: X response is generated for each valid function.

Q: Q response is generated for each valid function unless otherwise specified.

CAMAC FUNCTION CODES

F(1)•A(0): Read channel A programming word.

F(1)•A(1): Read channel B programming word.

F(9)•A(0): Stop channel A gate.

F(9)•A(1): Stop channel B gate.

F(17)•A(0): Write channel A programming word.

F(17)•A(1): Write channel B programming word.

F(25)•A(0): Start channel A gate.

F(25)•A(1): Start channel B gate.

Model 4222
Quad, Wide Range Gate and Delay Generator

CAMAC COMMANDS

Z: Initializes module, resets all channels, disables trigger input and enables CAMAC access (does not reset data registers).

C: Resets all channels (does not reset data registers) equivalent to front-panel Clear input.

I: Disables trigger input when present.

X: X response is generated for each valid function.

Q: Q response is generated for each valid function unless otherwise specified.

CAMAC FUNCTION CODES

F(0)•A(0-3): Reads selected program delay for channels 1-4 in 24 bits; Q = 1 always; 24-bit unsigned integer convention.

F(1)•A(0): Reads status via READ lines 1-4:
R1 = 1 if shortest delay elapsed;
R2 = 1 if longest delay elapsed;
R3 = 1 if Model 4222 is ready for trigger;
R4 = 1 if CAMAC access enabled.
All states are strobed by the leading edge of the CAMAC N signal.

F(9)•A(0): Resets all channels (does not reset data registers) equivalent to external Clear input.

F(16)•A(0-3): If CAMAC access enabled, writes delay to selected channel 1-4 in 24 bits. Q = 1 if CAMAC access enabled; Q = 0 otherwise. 24-bit unsigned integer convention.

F(24)•A(0): Disables unit; enables CAMAC access.

F(25)•A(0): Triggers the unit (OR'd with the external front-panel Trigger input):
Q = 1 if unit was ready for trigger;
Q = 0 otherwise.

F(26)•A(0): Enables unit; disables CAMAC access.